

FIG. 1A

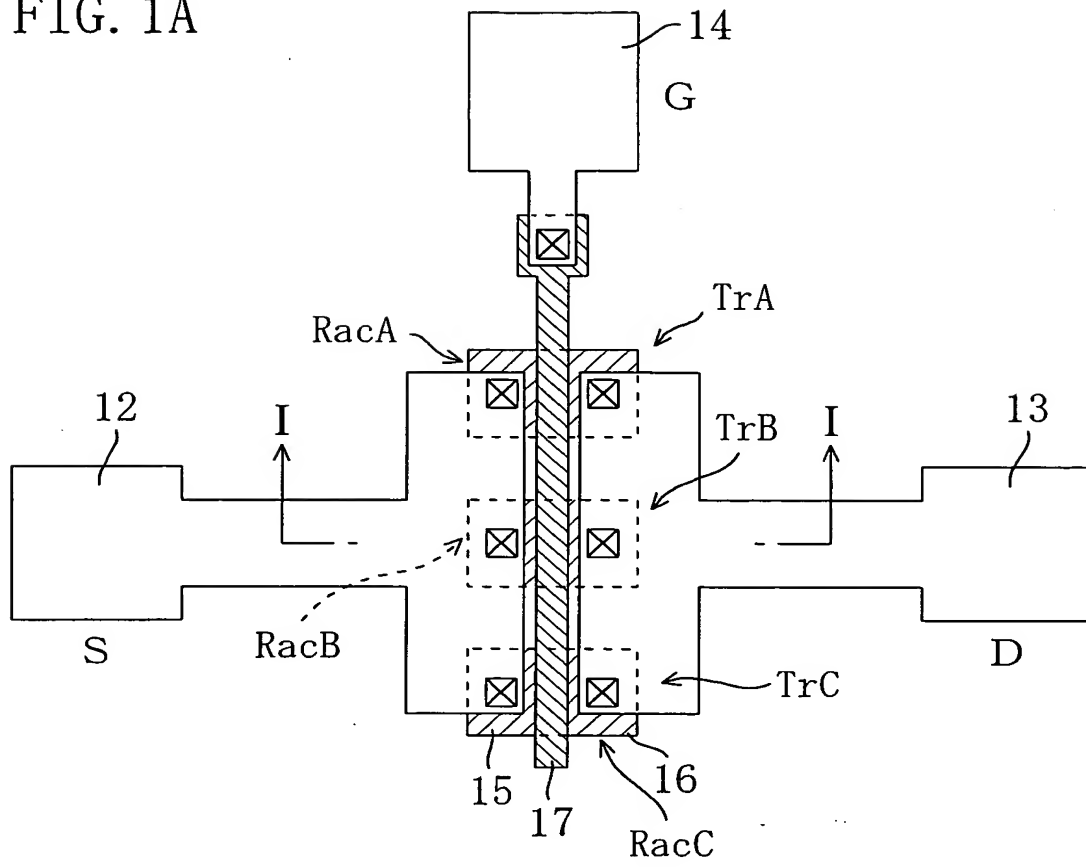


FIG. 1B

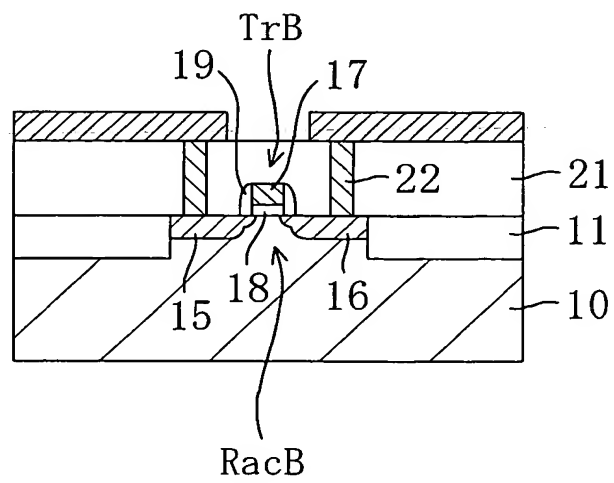


FIG. 2A

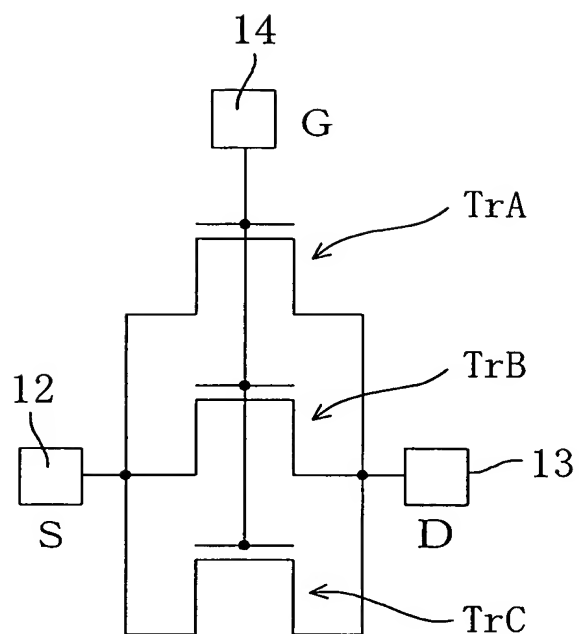


FIG. 2B

Characteristics of parallel-arranged MIS transistors used for evaluation are evaluated, and results are stored in memory.

ST10

Average value and variance of the values of the characteristics of the MIS transistors used for evaluation are calculated.

ST11

FIG. 3

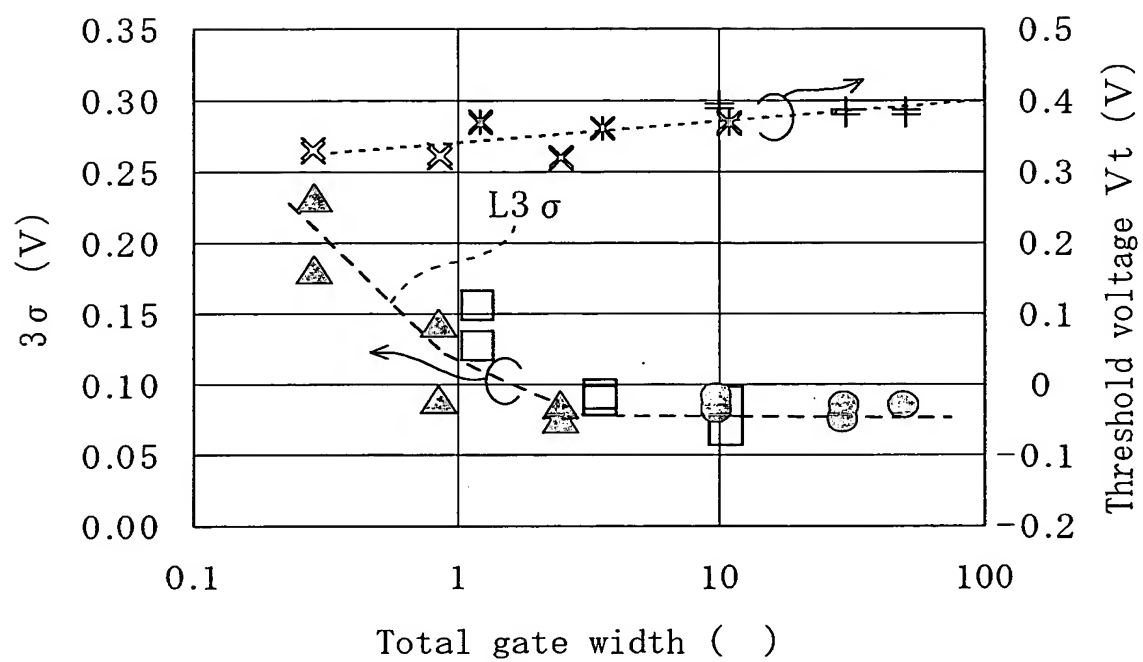


FIG. 4A

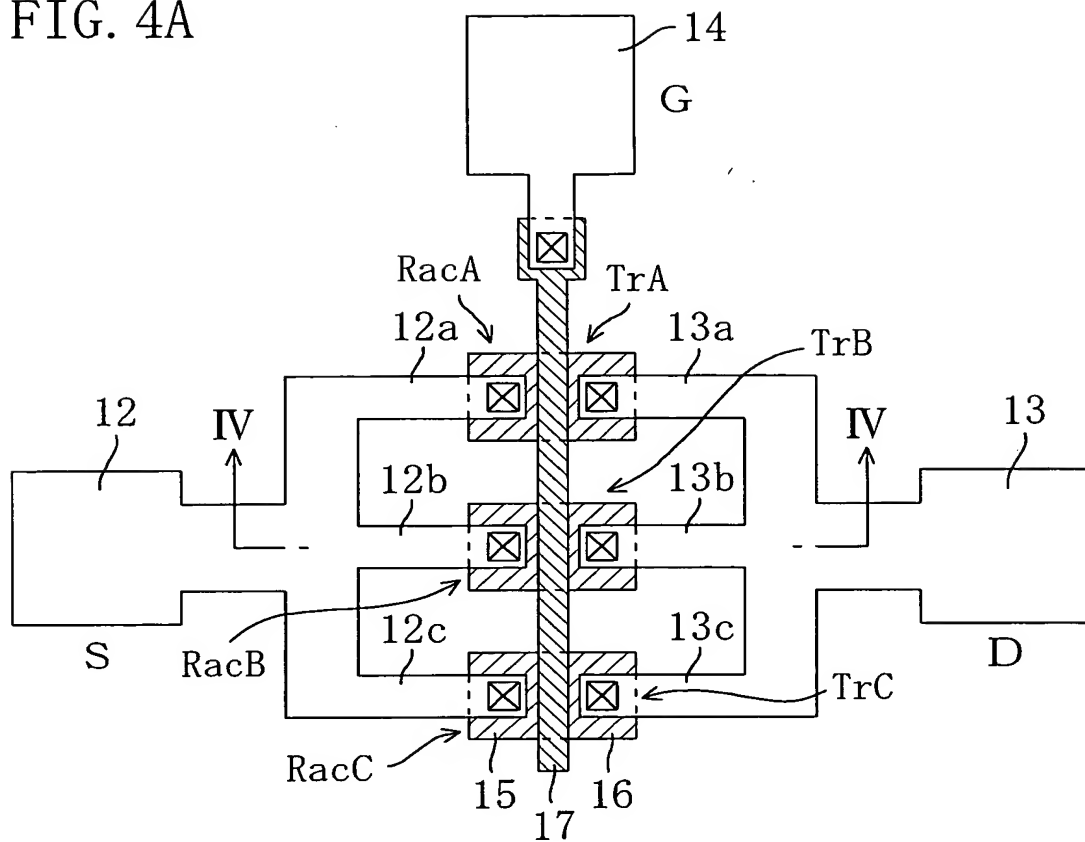


FIG. 4B

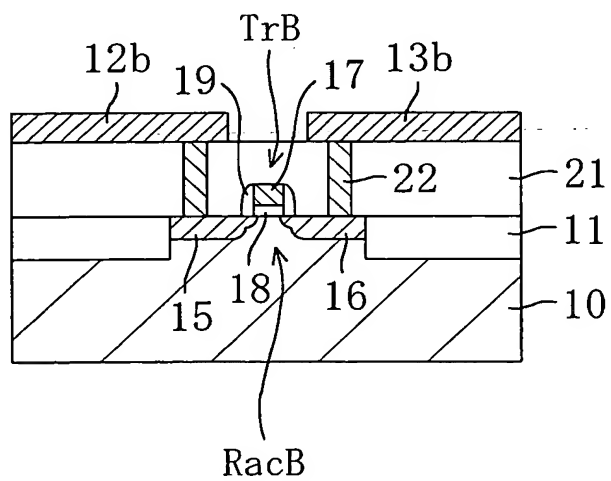


FIG. 5A

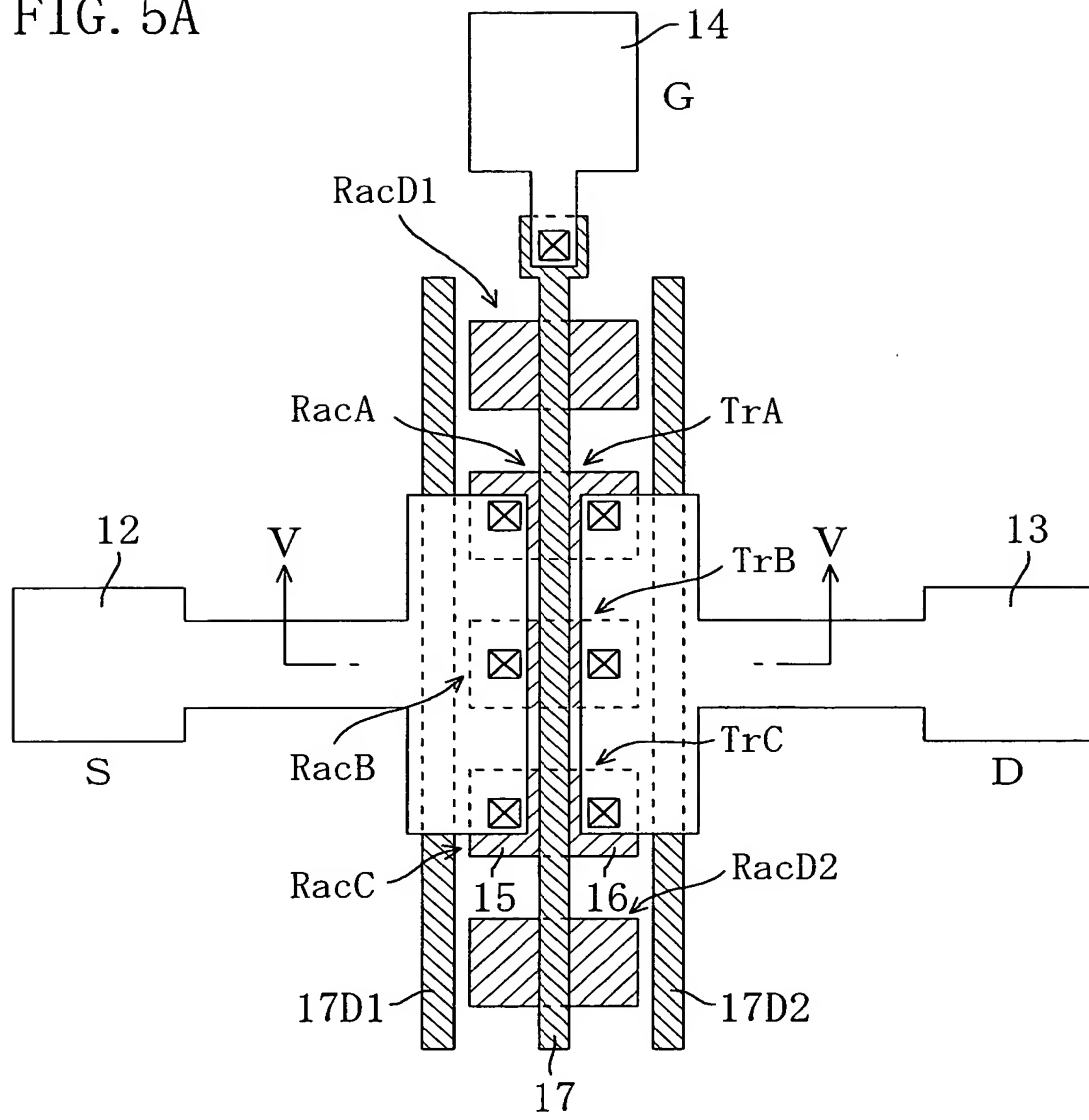


FIG. 5B

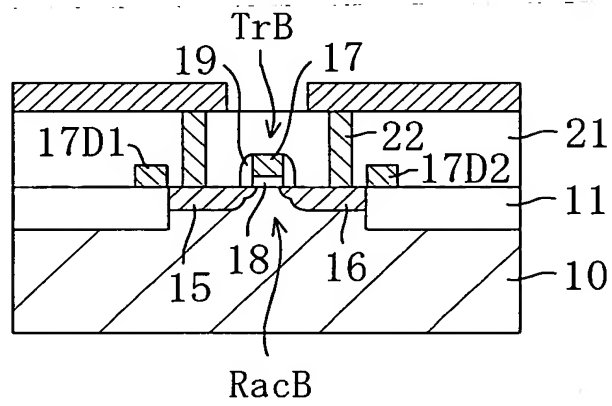


FIG. 6A

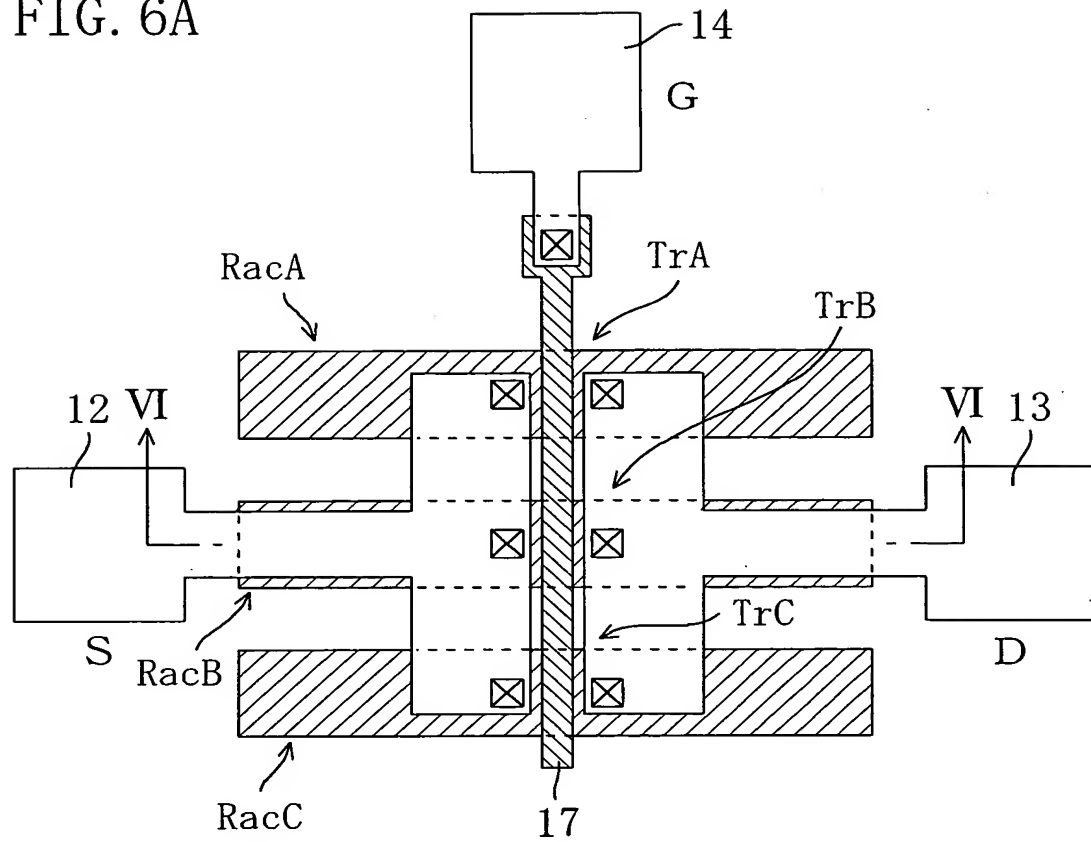
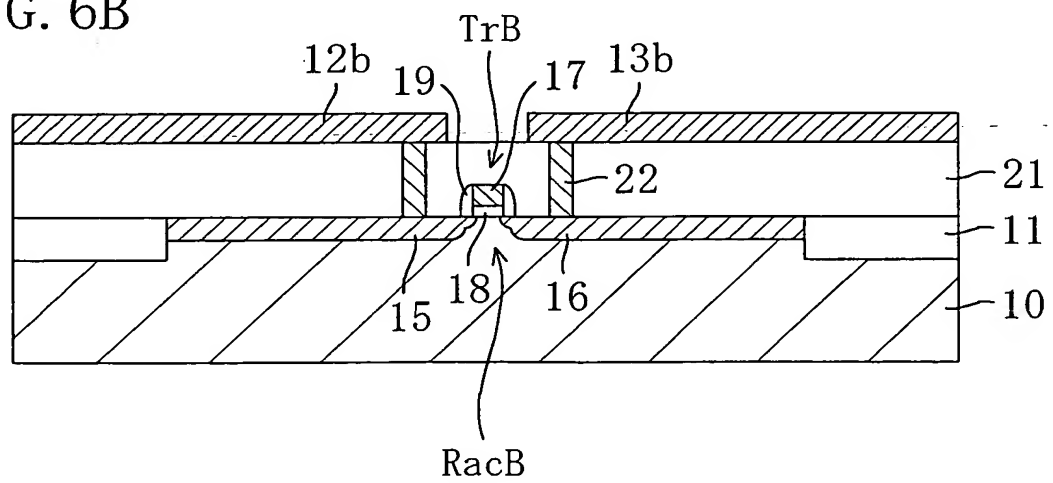


FIG. 6B



[illegible]

Fig. 1B is a cross-sectional view of a semiconductor device. It shows a central region with a gate stack (12, 12b, 19) and a contact (17) connected to a substrate (10) via a via (18). The device is surrounded by a passivation layer (13) and a trench (15). Labels include 10, 11, 12, 12b, 13, 15, 16, 17, 18, 19, 21, TrB, and RacB.

FIG. 8A

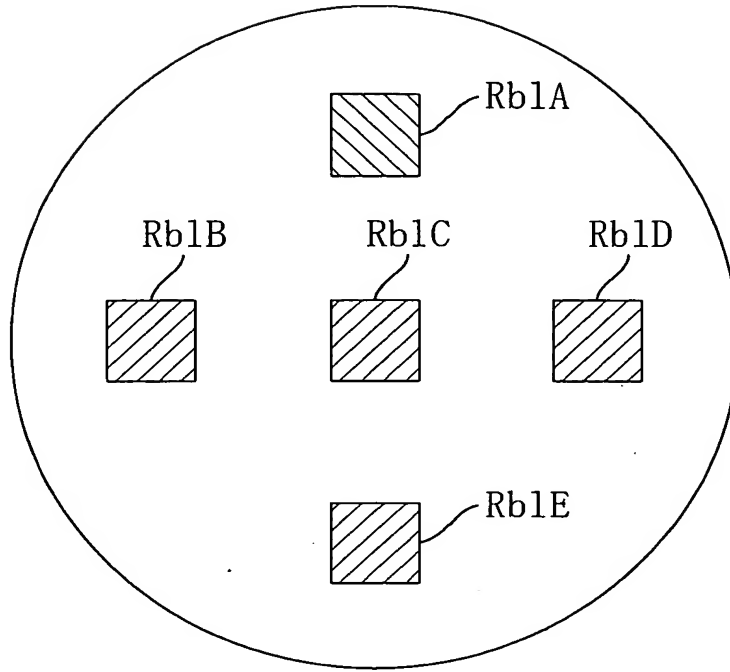


FIG. 8B

For each block, characteristics of single MIS transistors used for evaluation are evaluated, and results are stored in memory.



For each block, average value of the values of the characteristics of the MIS transistors used for evaluation is calculated, and result is stored in memory.



Average value and variance in wafer are calculated from the average values of the characteristics of the respective blocks.

FIG. 9

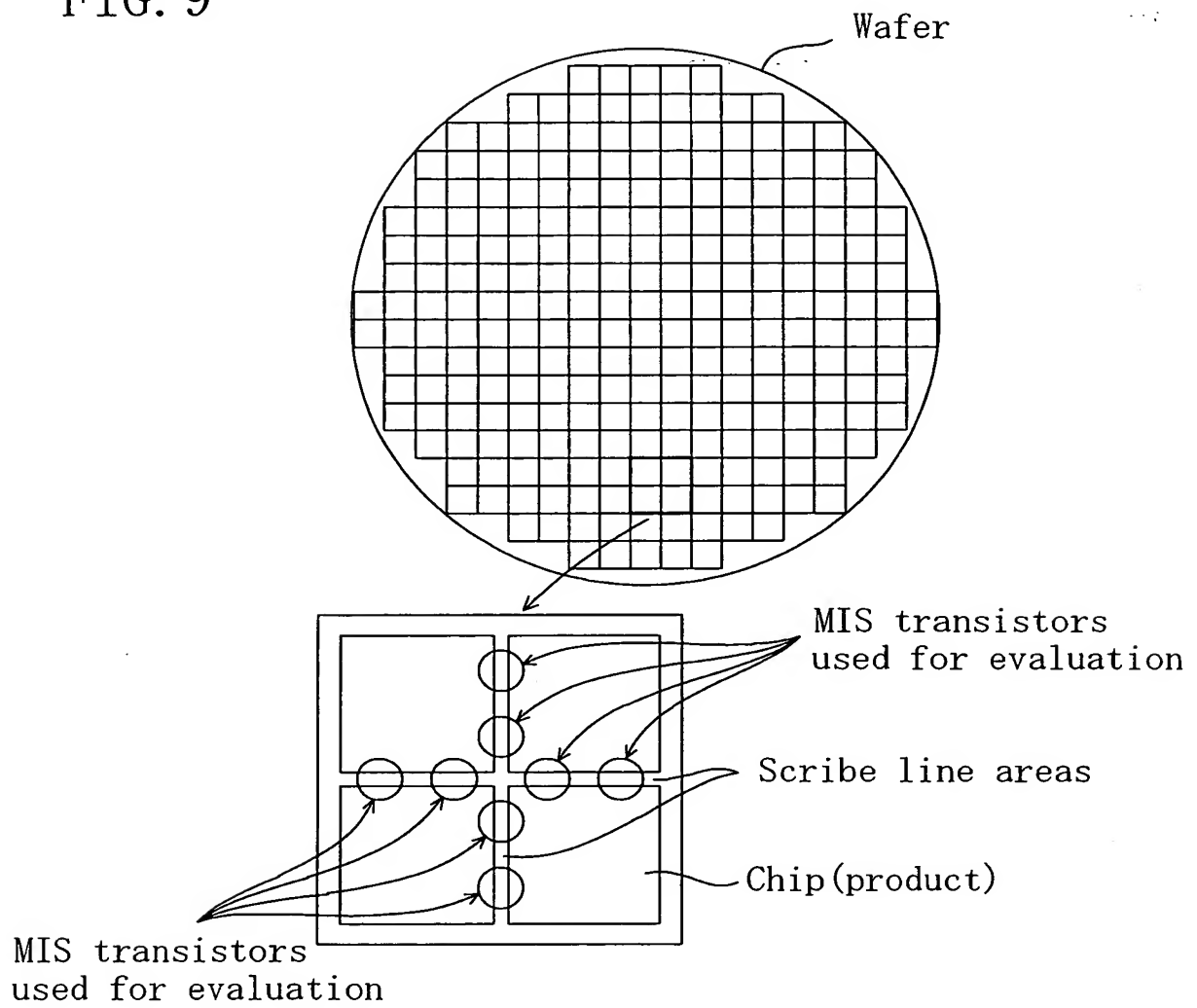


FIG. 10

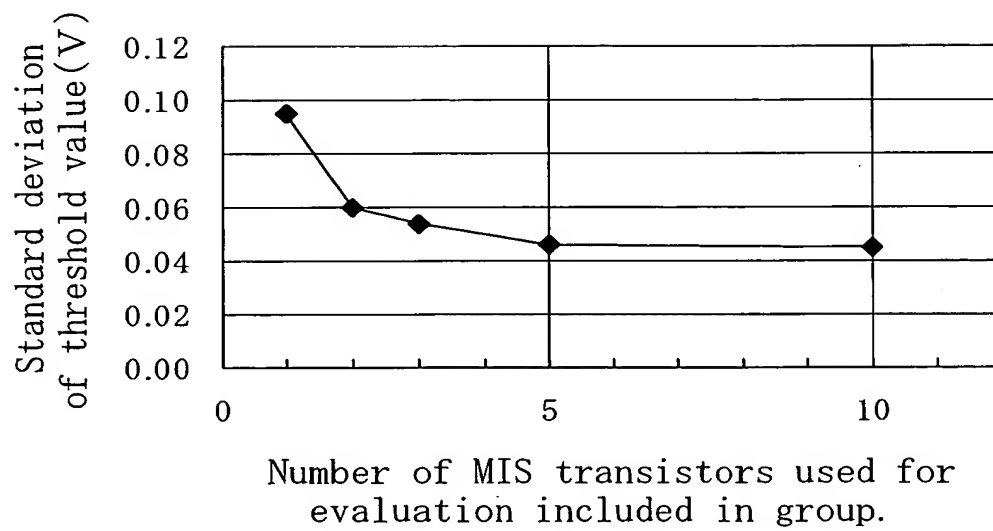


FIG. 11A
PRIOR ART

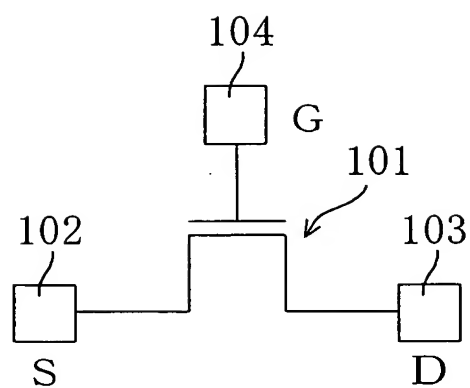


FIG. 11B
PRIOR ART

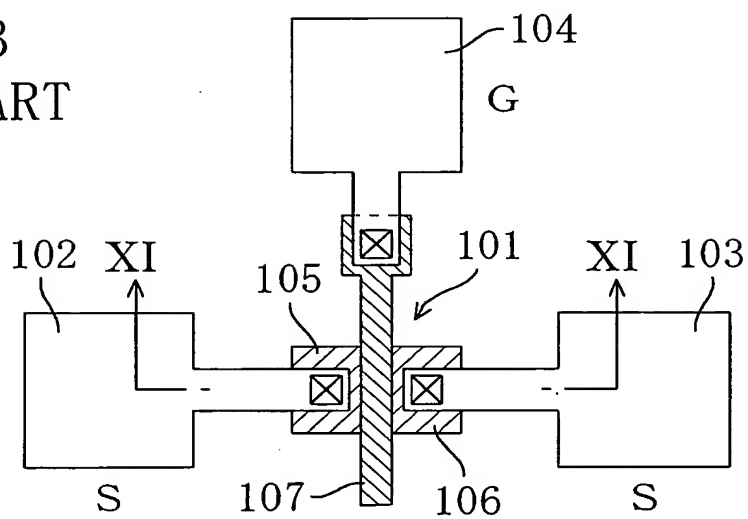


FIG. 11C
PRIOR ART

